Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the present application:

Listing of the Claims:

1-17. (Canceled).

18. (Currently amended) The integrated circuit device of Claim [[17]] 20 wherein the lower electrodes comprise semi-cylindrical lower electrodes symmetrically arranged in the intaglio pattern.

19. (Canceled).

20. (Currently amended) [[The]] An integrated circuit device ~~of Claim 19~~ comprising:

an integrated circuit substrate;

an interlayer dielectric on the integrated circuit substrate and having a plurality of buried contacts therein;

an oxide layer on the interlayer dielectric and having; an intaglio pattern ~~in the oxide layer~~ over the buried contacts;

a plurality of lower electrodes within a single opening in the intaglio pattern, the lower electrodes electrically contacting corresponding ones of the buried contacts; and

upper electrodes over corresponding lower electrodes interposing a ferroelectric layer therebetween, wherein the lower electrode, the ferroelectric layer and the upper electrode form a ferroelectric memory device;

wherein at least one of the lower electrodes comprises:

a horizontal electrode component contacting an upper surface of its corresponding buried contact; and

a vertical electrode component extending from the horizontal electrode component on a sidewall of the intaglio pattern.

21. (Currently amended) The integrated circuit device of Claim [[19]] 20 further comprising a plurality of transistors in the integrated circuit substrate and wherein the buried contacts electrically contact corresponding ones of the transistors.

22. (Currently amended) [[The]] An integrated circuit device ~~of Claim 19~~ comprising:

an integrated circuit substrate;

an interlayer dielectric on the integrated circuit substrate and having a plurality of buried contacts therein;

an oxide layer on the interlayer dielectric and having; an intaglio pattern ~~in the oxide layer~~ over the buried contacts;

a plurality of lower electrodes within a single opening in the intaglio pattern, the lower electrodes electrically contacting corresponding ones of the buried contacts; and

upper electrodes over corresponding lower electrodes interposing a ferroelectric layer therebetween, wherein the lower electrode, the ferroelectric layer and the upper electrode form a ferroelectric memory device;

wherein the intaglio pattern comprises a multi-step intaglio pattern extending along upper surfaces of the buried contacts and a part of sidewalls of the buried contacts.

23. (Previously presented) The integrated circuit device of Claim 22 wherein at least one of the lower electrodes comprises:

a first vertical electrode component extending along the part of the sidewall of its corresponding buried contact;

a horizontal electrode component extending from the first vertical electrode component along the upper surface of its corresponding buried contact; and

a second vertical electrode component extending from the horizontal electrode component along a sidewall of the multi-step intaglio pattern in the oxide layer.

24. (Original) The integrated circuit device of Claim 23 wherein the at least one of the lower electrodes further comprises a second horizontal electrode component extending inwardly from the first vertical electrode along a surface of the interlayer dielectric lower than a surface of the interlayer dielectric beyond the buried contacts.

25. (Original) The integrated circuit device of Claim 22 wherein the capacitors comprise semi-cylindrical capacitors symmetrically arranged in the intaglio pattern.

26-30. (Canceled).

31. (Previously presented) A ferroelectric memory device including semi-cylindrical capacitors, comprising:

an interlayer dielectric including at least two buried contacts;

an oxide layer formed on the interlayer dielectric;

a two-step intaglio pattern in the oxide layer and exposing upper surfaces and a part of sidewalls of the at least two buried contacts;

at least two lower electrodes formed in the two-step intaglio pattern, each of the at least two lower electrodes being in contact with a corresponding one of the at least two buried contacts; and

a ferroelectric layer and an upper electrode sequentially formed on the lower electrodes.

32. (Previously presented) The memory device of Claim 31 wherein a single opening in the intaglio pattern exposes the upper surfaces and the part of the sidewalls of the at least two buried contacts and wherein the at least two lower electrodes are formed in the single opening in the two-step intaglio pattern.

33. (Previously presented) The memory device of Claim 32 wherein at least one of the lower electrodes comprises:

a first vertical electrode component extending along the part of the sidewall of its corresponding buried contact;

a substantially planar horizontal electrode component extending directly from the first vertical electrode component along the upper surface of its corresponding buried contact; and

a second vertical electrode component extending directly from the horizontal electrode component along a sidewall of the multi-step intaglio pattern in the oxide layer.

34. (Previously presented) The memory device of Claim 32 wherein the upper surfaces of the at least two buried contacts are exposed by a first step of the intaglio pattern and the part of the sidewalls of the at least two buried contacts are exposed by a second step of the intaglio pattern extending between the at least two buried contacts.

35. (Canceled).